

NO Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-10 (Canceled)

11. (Previously Presented) A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the being two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode.

12. (Previously Presented) The refresh controller of claim 11 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

Claim 13 (Canceled)

14. (Previously Presented) The refresh controller of claim 11 wherein the reduced density mode comprises a half density mode.

Claims 15-26 (Canceled)

27. (Previously Presented) A dynamic random access memory (“DRAM”) comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the counter being two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented.

28. (Previously Presented) The dynamic random access memory of claim 27 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

Claims 29-35 (Canceled)

36. (Previously Presented) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the counter being two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented.

37. (Original) The computer system of claim 36 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

Claims 38-47 (Canceled)